

## 5.2.4 PLL Configuration

Table 5-2 shows the PLL configuration for the 750FX for nominal frequencies.

Table 5-2. 750FX Microprocessor PLL Configuration

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO Having an Example Range of...			
			SYSCLK <sup>6</sup> (MHz)		Core (MHz)	
Binary	Decimal		Minimum (SYSCLK <sub>MIN</sub> )	Maximum (SYSCLK <sub>MAX</sub> )	Minimum (Core Frequency <sub>MIN</sub> )	Maximum (Core Frequency <sub>MAX</sub> )
00000	0	OFF	N/A	N/A	Off	Off
00001	1	OFF	N/A	N/A	Off	Off
00010	2	PLL Bypass <sup>3</sup>	N/A	N/A	N/A	N/A
00011	3	PLL Bypass <sup>3</sup>	N/A	N/A	N/A	N/A
00100	4	2x <sup>1</sup>	—	—	—	—
00101	5	2.5x <sup>1</sup>	—	—	—	—
00110	6	3x	133	150 <sup>5</sup>	400	450
00111	7	3.5x	114	150 <sup>5</sup>	400	525
01000	8	4x	100	150 <sup>5</sup>	400	600
01001	9	4.5x	89	150 <sup>5</sup>	400	675
01010	10	5x	80	147	400	733
01011	11	5.5x	73	133	400	733
01100	12	6x	67	122	400	733
01101	13	6.5x	62	113	400	733
01110	14	7x	57	105	400	733
01111	15	7.5x	53	98	400	733
10000	16	8x	50	92	400	733
10001	17	8.5x	47	86	400	733
10010	18	9x	44	81	400	733
10011	19	9.5x	42	77	400	733
10100	20	10x	40	73	400	733
10101	21	11x	36 <sup>2</sup>	66	400	733
10110	22	12x	33 <sup>2</sup>	61	400	733

**Notes:**

1. The 2X- 2.5X Processor to Bus Ratios are currently not supported.
2. SYSCLK minimum is limited by the lowest frequency that manufacturing will support, see *Table 3-6 Clock AC Timing Specifications* on page 19 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.  
The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock-off mode, no clocking occurs inside the 750FX regardless of the SYSCLK input.
5. The SYSCLK limit is 150MHz, as specified in *Table 3-6* on page 19. Applications requiring SYSCLK over 150MHz must be investigated by application conditions.
6.  $SYSCLK = CoreFrequency / PBFR$   
The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PBFR).